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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,917	03/22/2004	Robert Tod Dimpsey	AUS920040063US1	3885

35525 7590 10/04/2007

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EXAMINER	
WANG, BEN C	
ART UNIT	PAPER NUMBER
2192	
MAIL DATE	DELIVERY MODE
10/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,917	DIMPSEY ET AL.	
	Examiner	Art Unit	
	Ben C. Wang	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,8-11,13,18-21 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,8-11,13,18-21 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment dated July 20, 2007, responding to the Office action mailed April 20, 2007 provided in the rejection of claims 1-26, wherein claims 1, 3, 8, 11, 13, 18, 21, and 23 are amended, claims 2, 4-7, 12, 14-17, 22, and 24-26 are canceled.

Claims 1, 3, 8-11, 13, 18-21, and 23 remain pending in the application and which have been fully considered by the examiner.

Applicant's arguments with respect to claims rejection have been fully considered but are moot in view of the new grounds of rejection – see both *Gover et al.* and *Johnston et al.*, arts made of record, as applied hereto.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Claim Rejections – 35 USC § 103(a)

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 8-11, 13, 18-21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gover et al. (Pat. No. 5,752,062) (hereinafter 'Gover' - art made of record) in view of Johnston et al. (Pat. No. US 6,212,675 B1) (hereinafter 'Johnston' - art made of record)

3. **As to claim 1** (Currently Amended), Gover discloses a method in a data processing system for presenting coverage data relating to data access occurring during execution of code, the method comprising:

- obtaining the coverage data containing data access indicators associated with memory locations (e.g., Fig. 5 – elements "63" – implement selected performance monitoring, "65" – collect selected performance monitoring data; Fig. 6A – Monitor Mode Control Register 0 (*MMCR0*); Col. 1, Lines 52-58 – Understanding the memory hierarchy behavior aids in developing algorithms that schedule and/or partition tasks, as well as distribut4 and structure data for optimizing the system; Lines 60-66 – The performance monitor produces

information relating to the utilization of a processor's instruction execution and storage control);

- identifying the data access indicators that have been set (e.g., Col. 8, Lines 42-50 – even .. to be recorded/counted, counter .. selection, counter freeze; Col. 10, Lines 53-63; Col. 11, Lines 14-50) by a processor in the data processing system in response to access of the memory locations during execution of the code by the processor to form set data access indicators, wherein each set data instruction access indicator is associated with a portion of the memory locations allocated for the code (e.g., Fig. 3 – FINISHED; Col. 20, Lines 48-65 – number ... branches dispatched .. completed; Col. 22, Lines 10-35 – *load* or *store*; Fig. 8 – a typical superscalar pipeline), and wherein the data access indicators are located in one of a shadow memory or a page table (e.g., Col. 8, Lines 26-39 – Note: special registers with state or content – *MMCRn* (Monitor Mode Control Registers) – maintained via special privilege access mode and being kept in parallel with execution scheduling – see Col. 11, Lines 14-50 – as informational support thereof, hence reads on shadowing type of information kept in memory; see Col. 9, Lines 36-57 – SSR (Saved State Register));
- identifying unset data access indicators that have remained unset during execution of the code by the processor (e.g., Col. 12, Lines 10-11 – once the enabled *IABR* match occurs, bit 29 of *MMCR1* is reset and counting occurs; Lines 19-21 – when an enabled *IABR* match occurs, hardware rests *PCUIABR* to zero and counting is enabled).

Gover does not explicitly disclose generating a presentation for coverage data in response to an event for identifying memory locations that have been accessed and for identifying memory locations that have not been accessed during execution of the code, wherein the set data access indicators and the unset data access indicators are identified in the presentation by one of using a first color to identify the set data access indicators and using a second color to identify the unset data access indicators, and using a graphical indicator to identify the set data access indicators and the unset data access indicators.

However, in an analogous art of Presentation of Visual Program Test Coverage Information, Johnston discloses generating a presentation for coverage data in response to an event for identifying memory locations that have been accessed and for identifying memory locations that have not been accessed during execution of the code, wherein the set data access indicators and the unset data access indicators are identified in the presentation by one of using a first color to identify the set data access indicators and using a second color to identify the unset data access indicators, and using a graphical indicator to identify the set data access indicators and the unset data access indicators (e.g., Col. 1, Lines 62 through Col. 2, Lines 15 – "Optionally, the means for visually indicating further comprises using a first color for each of the elements having the element test coverage status which indicates covered, and a second color for each of the elements having the element test coverage status which indicates not covered" (emphasis added)).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Gover into the Johnston's system to further provide generating a presentation for coverage data in response to an event for identifying memory locations that have been accessed and for identifying memory locations that have not been accessed during execution of the code, wherein the set data access indicators and the unset data access indicators are identified in the presentation by one of using a first color to identify the set data access indicators and using a second color to identify the unset data access indicators, and using a graphical indicator to identify the set data access indicators and the unset data access indicators in Gover system.

The motivation is that it would further enhance the Gover's system by taking, advancing and/or incorporating Johnston's system which offers significant advantages for providing a technique for presenting test coverage metrics for a visual program in a manner that is familiar to the visual programmer, and providing this additional information using color, line thickness, line style, added text, or other graphical representations as once suggested by Johnston (e.g., Summary of the Invention, Lines 29-43).

4. **As to claim 3** (incorporating the rejection in claim 1) (Currently Amended), Johnston discloses the method wherein the event is completion of the execution of the code, and further comprising:

- receiving new test parameters after generating the presentation (e.g., Col. 6, Lines 46-49 – the input parameter is obtained from input data that the-user will enter using the entry filed in New Item part 320, which is then passed as a parameter of connection 312); and
- in response to receiving the new test parameters, repeating the obtaining step, the identifying steps, and the generating step (e.g., Fig. 4 – element 430 – "Wait for user action", 410 – "User selects part, and optionally category and element", 420 – "Display coverage information, with detail fro lowest selected level").

5. **As to claim 8** (incorporating the rejection in claim 1) (Currently Amended), Gover discloses the method wherein the event is at least one of a completion of the execution of the code (e.g., Fig. 8 – element of "COMPLETION"), expiration of a time (e.g., Col. 8, Lines 56-65 – The performance monitor 50 is provided in conjunction with a time base facility 52 which includes a counter that designates a precise point in time for saving the machine state), and the execution of a selected type of instruction in the code (e.g., Fig. 2 – "INSTRUCTION TYPE", element 76 – "RECORDER BUFFER"; Col. 6, Line 66 through Col. 7, Line 2 – Each entry has five primary fields, namely an "instruction type" field, ...).

6. **As to claim 9** (incorporating the rejection in claim 1) (Original), Gover discloses the method wherein the portion of the memory locations is a single memory location in the code and wherein every memory location in the memory locations is associated with

a different data access indicator (e.g., Fig. 6A – Monitor Mode control Register 0 (*MMCR0*); Fig. 6B – *MMCR1*; Col. 3, Lines 24-25 - Figs. 6a and 6b illustrate monitor mode control registers (*MMCRn*) utilized to manage a plurality of counters).

7. **As to claim 10** (incorporating the rejection in claim 1) (Original), Gover discloses the method wherein the portion of the memory locations includes at least one of a memory area or a single memory location (e.g., Col. 1, Lines 52-58 – Studies of a program's access patterns to memory and interaction with a system's memory hierarchy are performed to determine system efficiency; Col. 13, Lines 17-20 – the data address breakpoint register (DABR) will be defined as a register that contains an effective address that is used to compare to the address belonging to a memory access).

8. **As to claim 11** (Currently Amended), Gover discloses a data processing system for presenting coverage data relating to data access occurring during execution of code, the data processing system comprising:

- obtaining means for obtaining the coverage data containing data access indicators associated with memory locations (e.g., Fig. 5 – elements "63" – implement selected performance monitoring, "65" – collect selected performance monitoring data; Fig. 6A – Monitor Mode Control Register 0 (*MMCR0*); Col. 1, Lines 52-58 – Understanding the memory hierarchy behavior aids in developing algorithms that schedule and/or partition tasks, as well as distribut4 and structure data for optimizing the system; Lines 60-66 – The performance monitor produces

information relating to the utilization of a processor's instruction execution and storage control);

- first identifying means for identifying the data access indicators that have been set (e.g., Col. 8, Lines 42-50 – even .. to be recorded/counted, counter .. selection, counter freeze; Col. 10, Lines 53-63; Col. 11, Lines 14-50) by a processor in the data processing system in response to access of the memory locations during execution of the code by the processor to form set data access indicators, wherein each set instruction data access indicator is associated with a portion of the memory locations allocated for the code (e.g., Fig. 3 – FINISHED; Col. 20, Lines 48-65 – number ... branches dispatched .. completed; Col. 22, Lines 10-35 – *load* or *store*; Fig. 8 – a typical superscalar pipeline), and wherein the data access indicators are located in one of a shadow memory or a page table (e.g., Col. 8, Lines 26-39 – Note: special registers with state or content – *MMCRn* (Monitor Mode Control Registers) – maintained via special privilege access mode and being kept in parallel with execution scheduling – see Col. 11, Lines 14-50 – as informational support thereof, hence reads on shadowing type of information kept in memory; see Col. 9, Lines 36-57 – SSR (Saved State Register));
- second identifying means for identifying unset data access indicators that have remained unset during execution of the code by the processor (e.g., Col. 12, Lines 10-11 – once the enabled *IABR* match occurs, bit 29 of *MMCR1* is reset

and counting occurs; Lines 19-21 – when an enabled *IABR* match occurs, hardware rests *PCUIABR* to zero and counting is enabled).

Gover does not explicitly disclose generating means for generating a presentation for coverage data in response to an event for identifying memory locations that have been accessed and for identifying memory locations that have not been accessed during execution of the code, wherein the set data access indicators and the unset data access indicators are identified in the presentation by one of using a first color to identify the set data access indicators and using a second color to identify the unset data access indicators, and using a graphical indicator to identify the set data access indicators and the unset data access indicators.

However, in an analogous art of Presentation of Visual Program Test Coverage Information, Johnston discloses generating means for generating a presentation for coverage data in response to an event for identifying memory locations that have been accessed and for identifying memory locations that have not been accessed during execution of the code, wherein the set data access indicators and the unset data access indicators are identified in the presentation by one of using a first color to identify the set data access indicators and using a second color to identify the unset data access indicators, and using a graphical indicator to identify the set data access indicators and the unset data access indicators (e.g., Col. 1, Lines 62 through Col. 2, Lines 15 – "Optionally, the means for visually indicating further comprises using a first color for each of the elements having the element test coverage status which indicates covered,

and a second color for each of the elements having the element test coverage status which indicates not covered" (emphasis added)).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Gover into the Johnston's system to further provide generating means for generating a presentation for coverage data in response to an event for identifying memory locations that have been accessed and for identifying memory locations that have not been accessed during execution of the code, wherein the set data access indicators and the unset data access indicators are identified in the presentation by one of using a first color to identify the set data access indicators and using a second color to identify the unset data access indicators, and using a graphical indicator to identify the set data access indicators and the unset data access indicators in Gover system.

The motivation is that it would further enhance the Gover's system by taking, advancing and/or incorporating Johnston's system which offers significant advantages for providing a technique for presenting test coverage metrics for a visual program in a manner that is familiar to the visual programmer, and providing this additional information using color, line thickness, line style, added text, or other graphical representations as once suggested by Johnston (e.g., Summary of the Invention, Lines 29-43).

9. **As to claim 13** (incorporating the rejection in claim 11) (Currently Amended), please refer to claim **3** above accordingly.

10. **As to claim 18** (incorporating the rejection in claim 11) (Currently Amended), please refer to claim **8** above accordingly.

11. **As to claim 19** (incorporating the rejection in claim 11) (Original), please refer to claim **9** above accordingly.

12. **As to claim 20** (incorporating the rejection in claim 11) (Original), please refer to claim **10** above accordingly.

13. **As to claim 21** (Currently Amended), Gover discloses a computer program product in a recordable-type computer readable medium for presenting coverage data relating to data access occurring during execution of code, the computer program product comprising:

- first instructions for obtaining the coverage data containing data access indicators associated with memory locations (e.g., Fig. 5 – elements "63" – implement selected performance monitoring, "65" – collect selected performance monitoring data; Fig. 6A – Monitor Mode Control Register 0 (*MMCR0*); Col. 1, Lines 52-58 – Understanding the memory hierarchy behavior aids in developing algorithms that schedule and/or partition tasks, as well as distribut4 and structure data for optimizing the system; Lines 60-66 – The performance monitor produces information relating to the utilization of a processor's instruction execution and storage control);

- second instructions for identifying the data access indicators that have been set (e.g., Col. 8, Lines 42-50 – even .. to be recorded/counted, counter .. selection, counter freeze; Col. 10, Lines 53-63; Col. 11, Lines 14-50) by a processor in the data processing system in response to access of the memory locations during execution of the code by the processor to form set data access indicators, wherein each set instruction data access indicator is associated with a portion of the memory locations allocated for the code (e.g., Fig. 3 – FINISHED; Col. 20, Lines 48-65 – number ... branches dispatched .. completed; Col. 22, Lines 10-35 – *load* or *store*; Fig. 8 – a typical superscalar pipeline), and wherein the data access indicators are located in one of a shadow memory or a page table (e.g., Col. 8, Lines 26-39 – Note: special registers with state or content – *MMCRn* (Monitor Mode Control Registers) – maintained via special privilege access mode and being kept in parallel with execution scheduling – see Col. 11, Lines 14-50 – as informational support thereof, hence reads on shadowing type of information kept in memory; see Col. 9, Lines 36-57 – SSR (Saved State Register));
- third instructions for identifying unset data access indicators that have remained unset during execution of the code by the processor (e.g., Col. 12, Lines 10-11 – once the enabled *IABR* match occurs, bit 29 of *MMCR1* is reset and counting occurs; Lines 19-21 – when an enabled *IABR* match occurs, hardware rests *PCUIABR* to zero and counting is enabled).

Gover does not explicitly disclose fourth instructions for generating a presentation for coverage data in response to an event for identifying memory locations that have been

accessed and for identifying memory locations that have not been accessed during execution of the code, wherein the set data access indicators and the unset data access indicators are identified in the presentation by one of using a first color to identify the set data access indicators and using a second color to identify the unset data access indicators, and using a graphical indicator to identify the set data access indicators and the unset data access indicators.

However, in an analogous art of Presentation of Visual Program Test Coverage Information, Johnston discloses fourth instructions for generating a presentation for coverage data in response to an event for identifying memory locations that have been accessed and for identifying memory locations that have not been accessed during execution of the code, wherein the set data access indicators and the unset data access indicators are identified in the presentation by one of using a first color to identify the set data access indicators and using a second color to identify the unset data access indicators, and using a graphical indicator to identify the set data access indicators and the unset data access indicators (e.g., Col. 1, Lines 62 through Col. 2, Lines 15 – "Optionally, the means for visually indicating further comprises using a first color for each of the elements having the element test coverage status which indicates covered, and a second color for each of the elements having the element test coverage status which indicates not covered" (emphasis added)).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Gover into the Johnston's system to further provide fourth instructions for generating a presentation for coverage

data in response to an event for identifying memory locations that have been accessed and for identifying memory locations that have not been accessed during execution of the code, wherein the set data access indicators and the unset data access indicators are identified in the presentation by one of using a first color to identify the set data access indicators and using a second color to identify the unset data access indicators, and using a graphical indicator to identify the set data access indicators and the unset data access indicators in Gover system.

The motivation is that it would further enhance the Gover's system by taking, advancing and/or incorporating Johnston's system which offers significant advantages for providing a technique for presenting test coverage metrics for a visual program in a manner that is familiar to the visual programmer, and providing this additional information using color, line thickness, line style, added text, or other graphical representations as once suggested by Johnston (e.g., Summary of the Invention, Lines 29-43).

14. **As to claim 23** (incorporating the rejection in claim 21) (Currently Amended), please refer to claim **3** above accordingly.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben C. Wang whose telephone number is 571-270-1240. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TUAN DAM
SUPERVISORY PATENT EXAMINER

BCW

September 12, 2007